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AUTOMATIC TEST PATTERN GENERATION FOR FUNCTIONAL REGISTER
TRANSFER LEVEL CIRCUITS USING ASSIGNMENT DECISION DIAGRAMS

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ABSTRACT

Test patterns are generated by generating assignment decision diagrams that represent a register transfer level digital circuit. A nine-valued symbolic algebra is used in which objectives are determined for portions identified in the assignment decision diagram. The objectives are justified and propagated by traversing the assignment decision diagram in which a test environment is found. Heuristics are used if a test environment is not initially found. Using the test environment found, predetermined test vectors are propagated to obtain a system-level test set. Each test set for each portion are concatenated to obtain a complete test set for the register transfer level digital circuit.

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